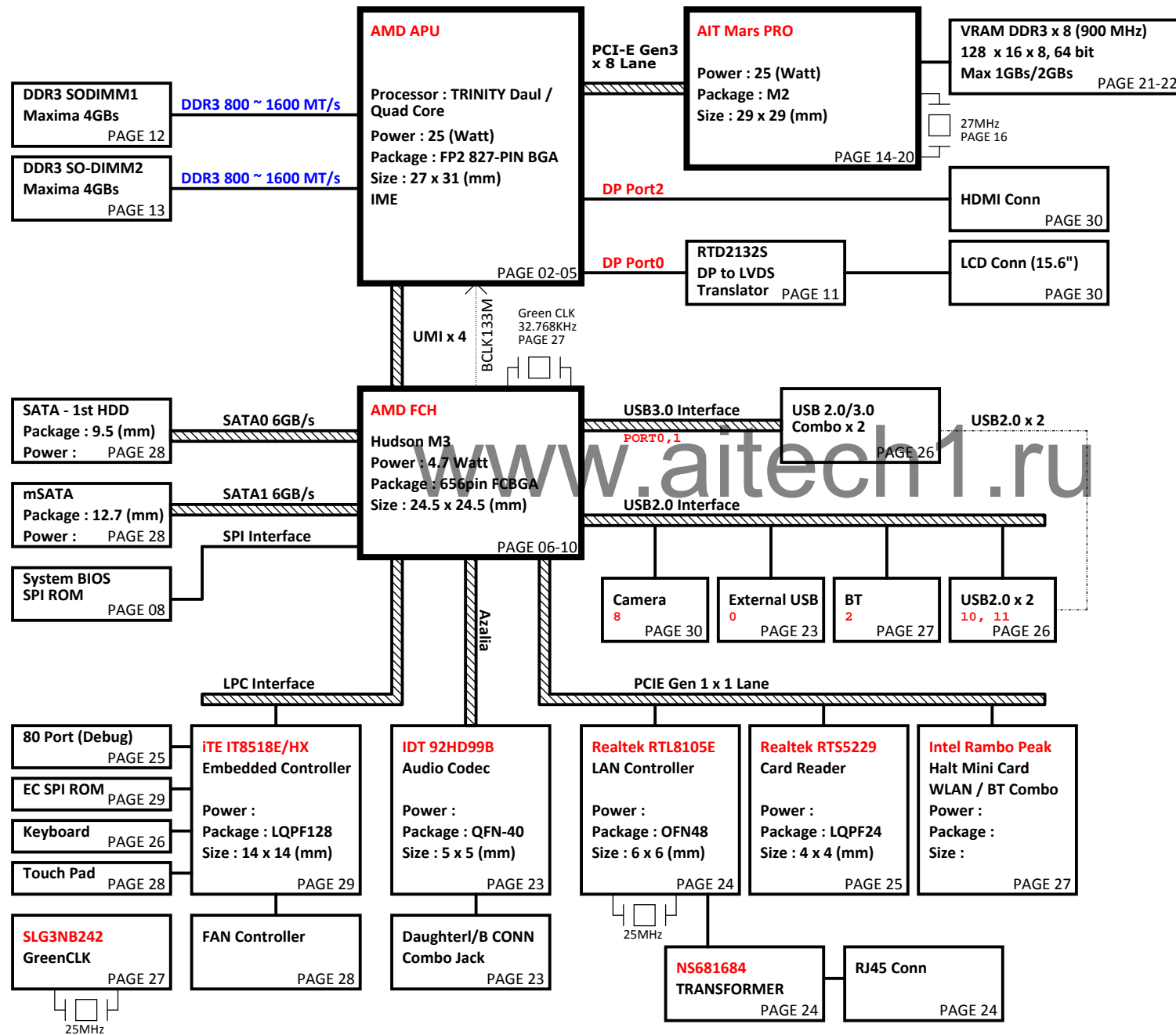


Volks_AMD Comal DIS/UMA (14") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLAVCC/+1.1V)

Richtek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

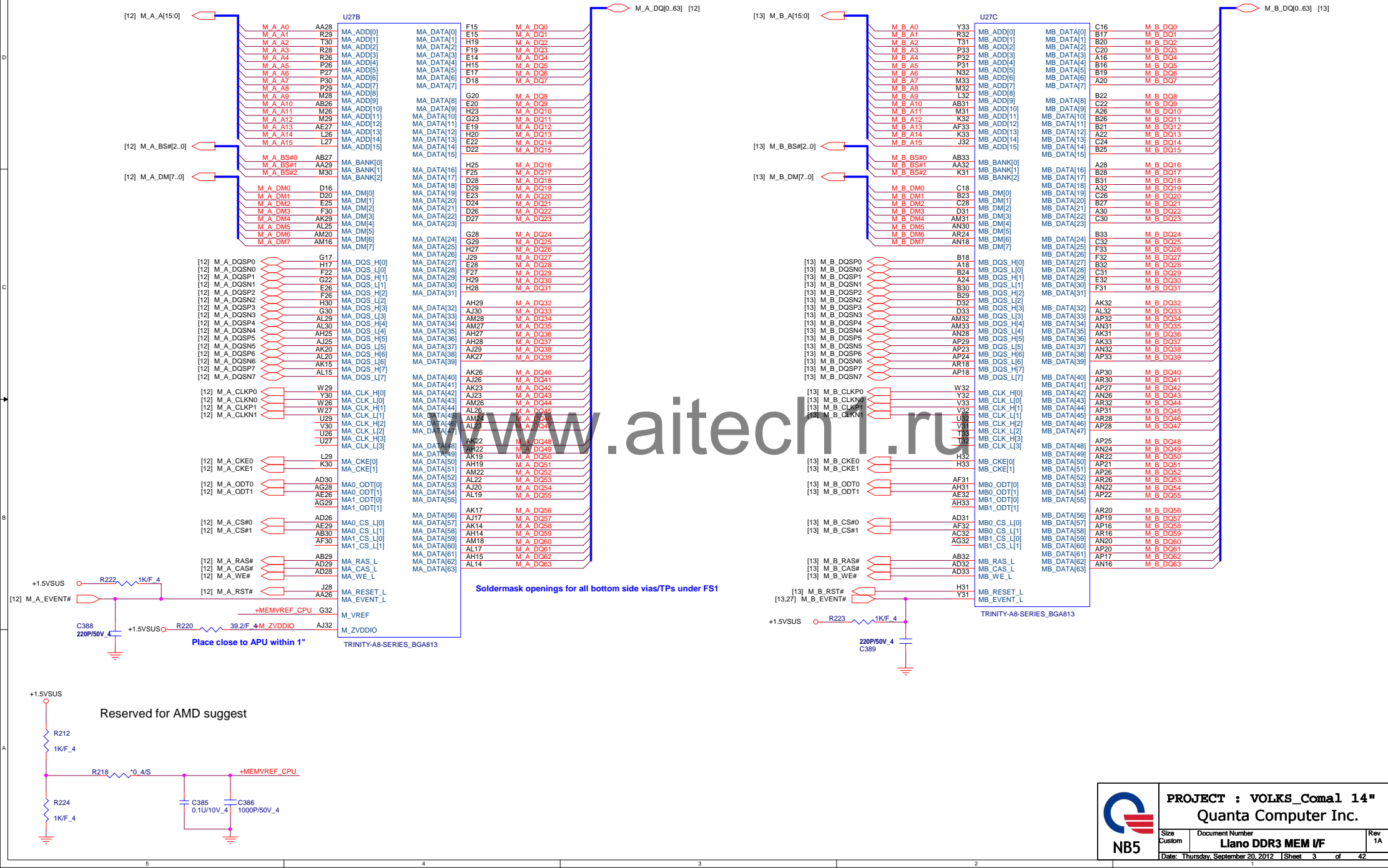
Richtek RT8228AZ
PCH Power (+1.1VS5)

RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

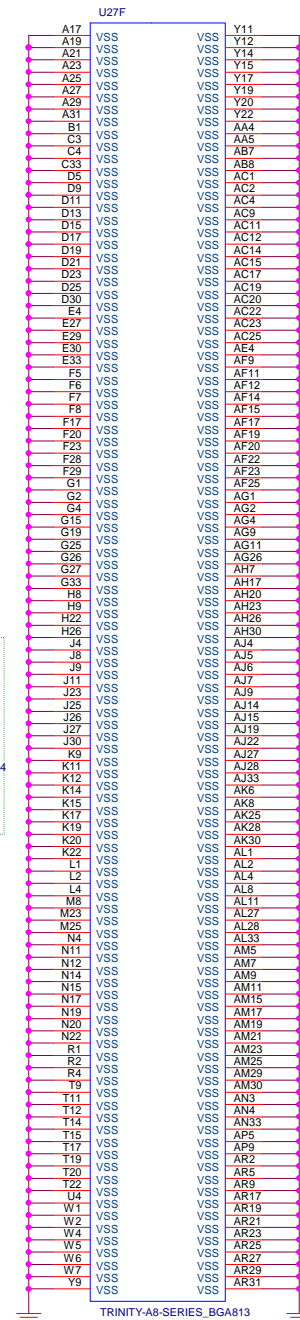
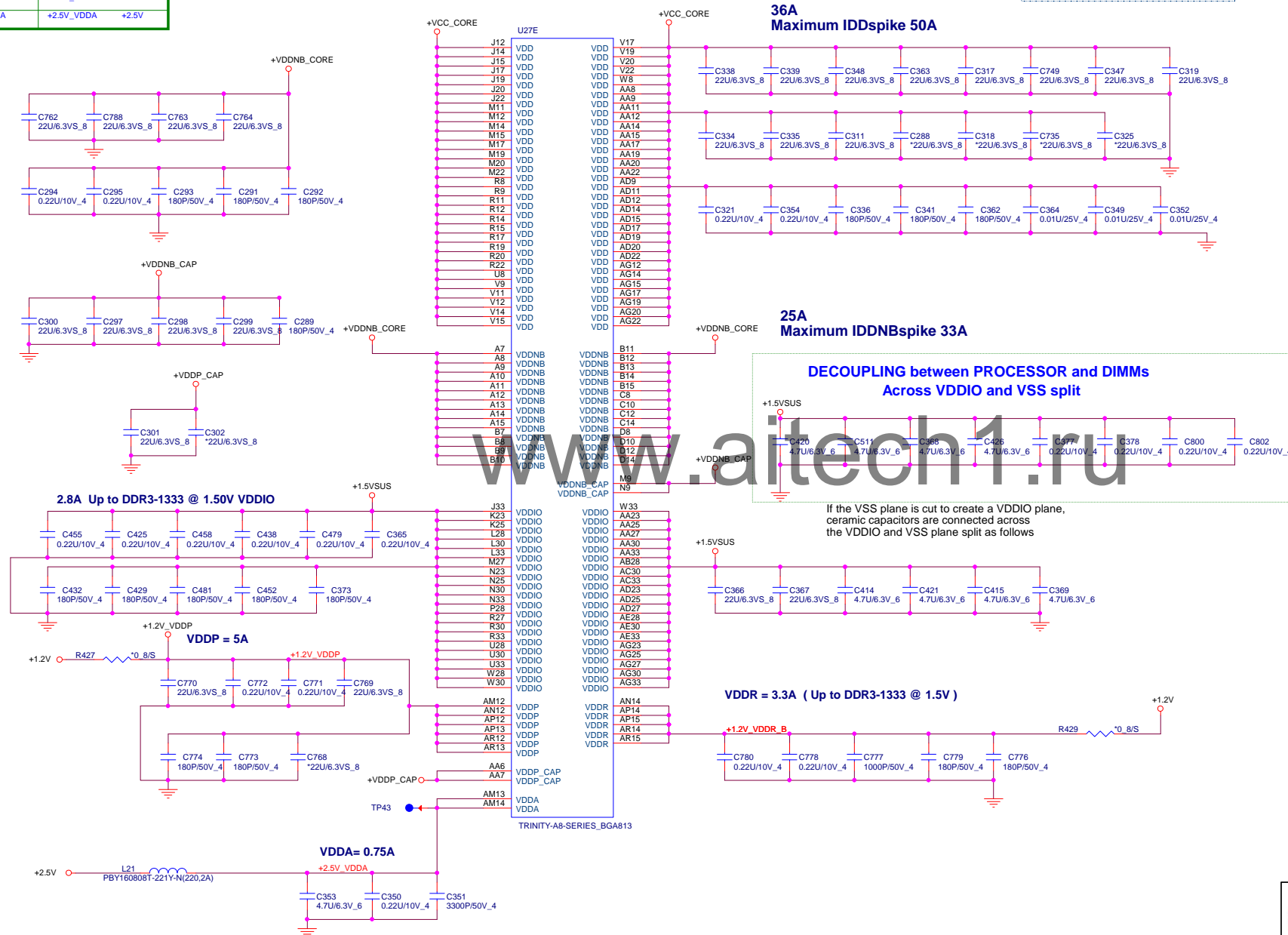
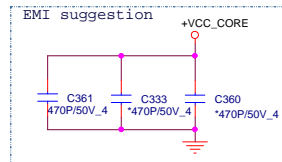
Size A3 Document Number Rev 1A
Block Diagram
Date: Thursday, September 20, 2012 1 Sheet 1 of 42



	R
--	----------

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

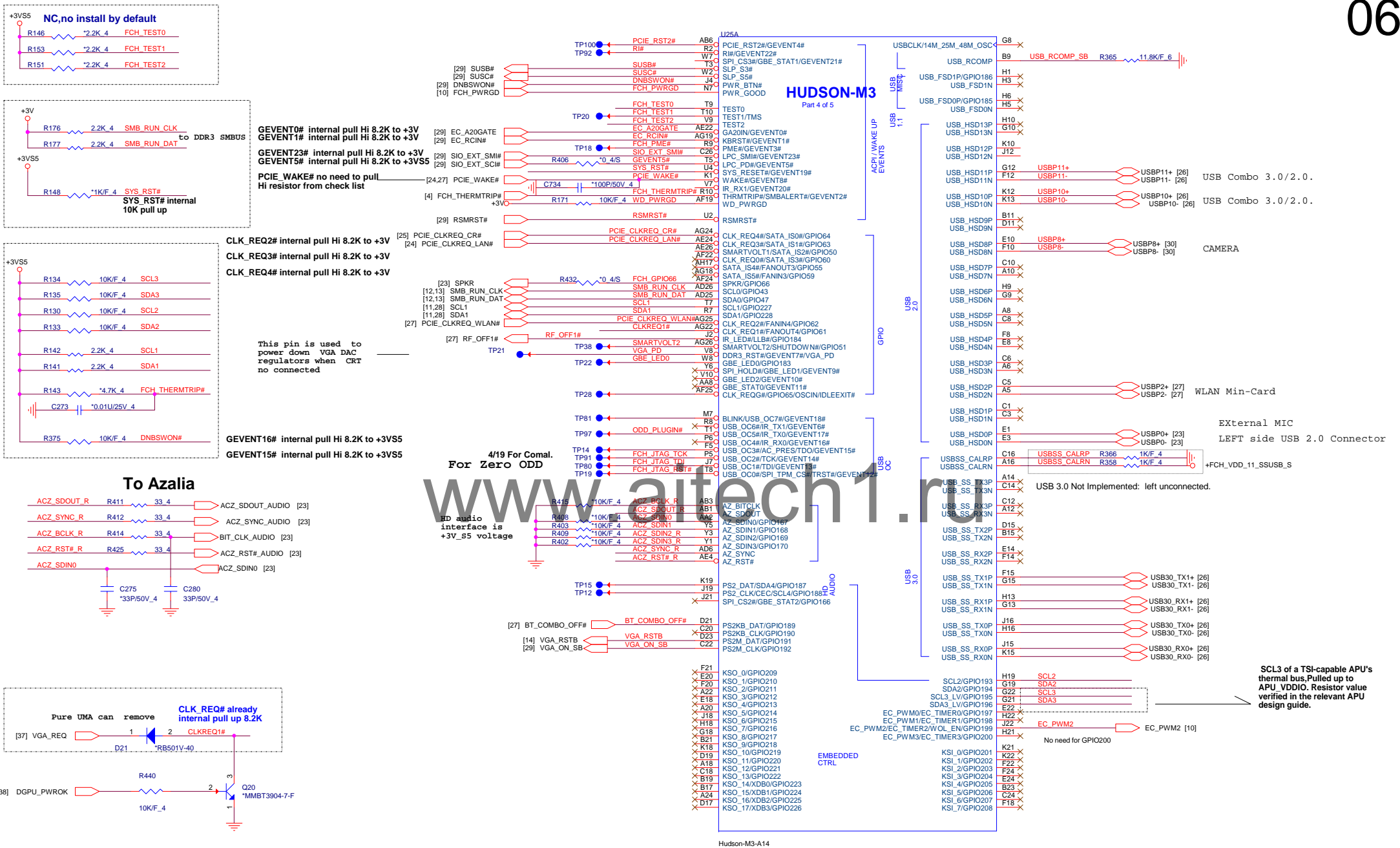


PROJECT : VOLKS_Comal 14"

Quanta Computer Inc.

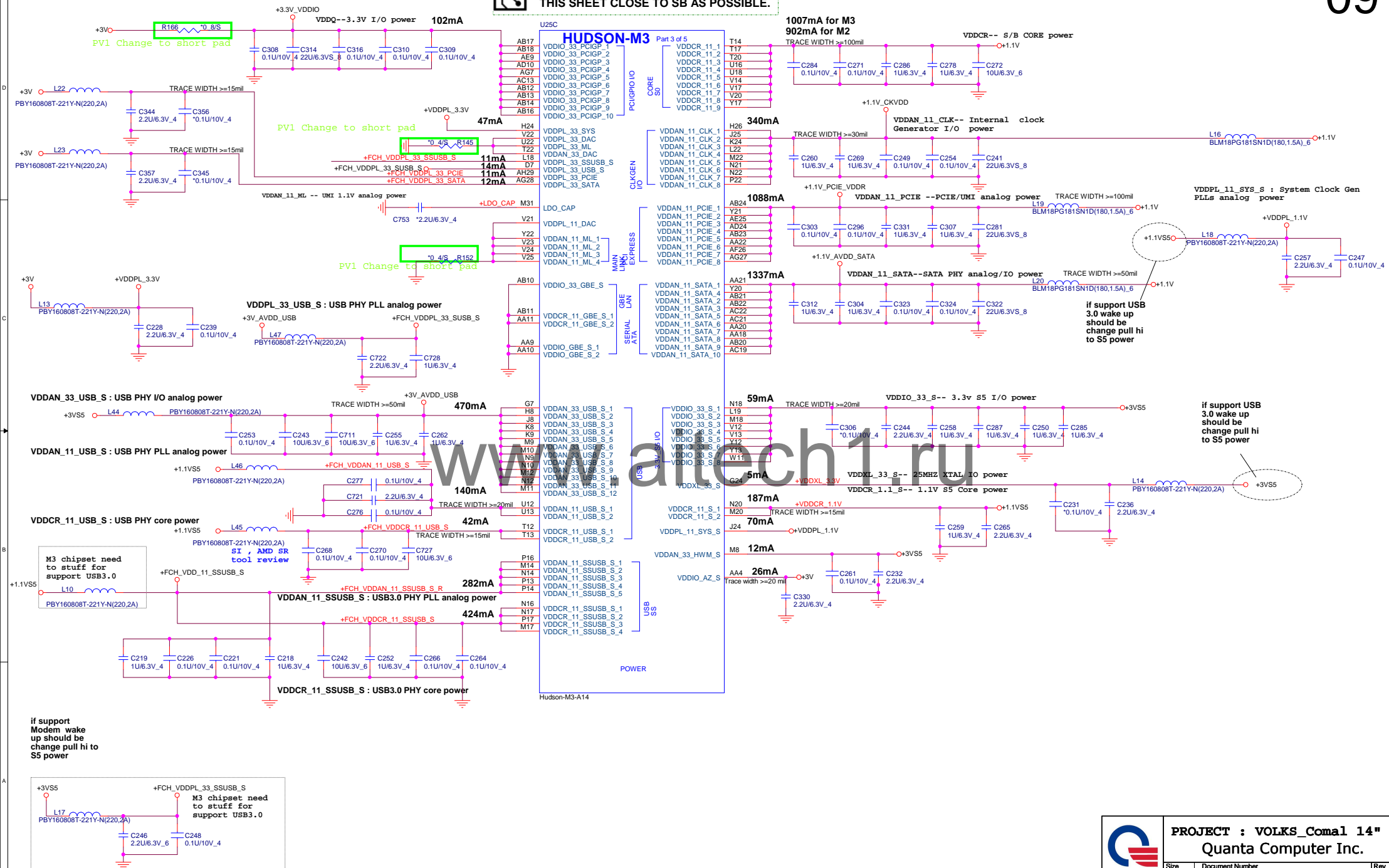
Size Custom Document Number Liano POWER/GND Rev 1A

Date: Thursday, September 20, 2012 1 Sheet 5 of 42





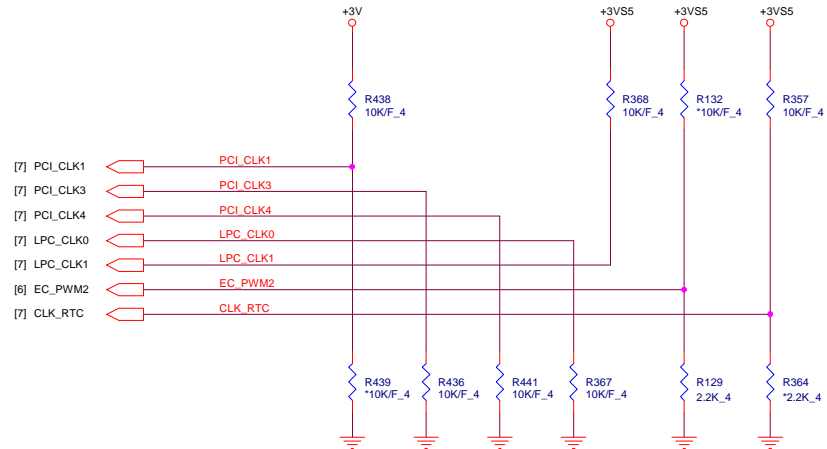
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

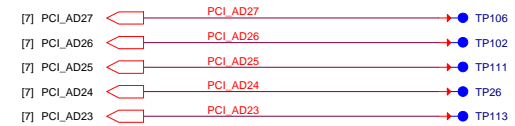


REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

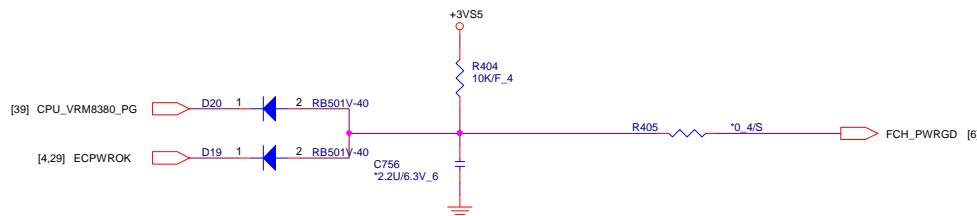
FCH has 15K Internal Pull Up for PCI_AD[27:23]

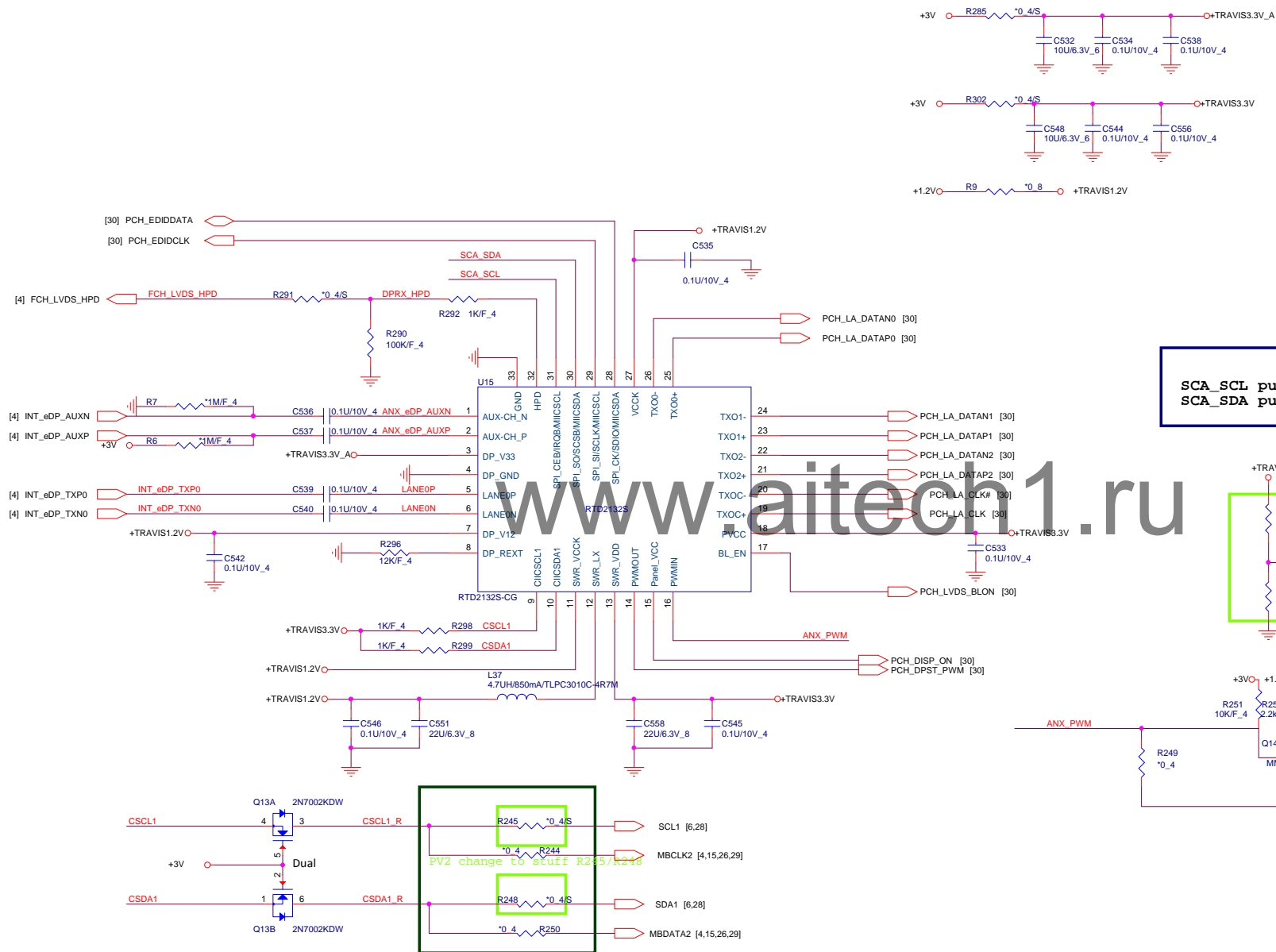


remove reserve pull low resistor
reserve test point only.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

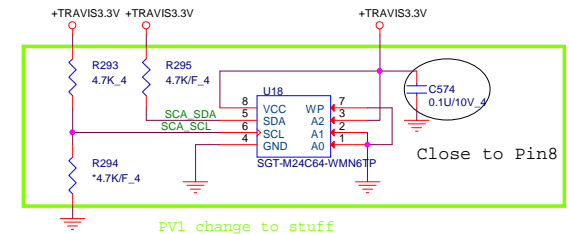
FCH_PWRGD

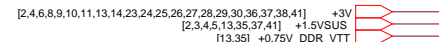


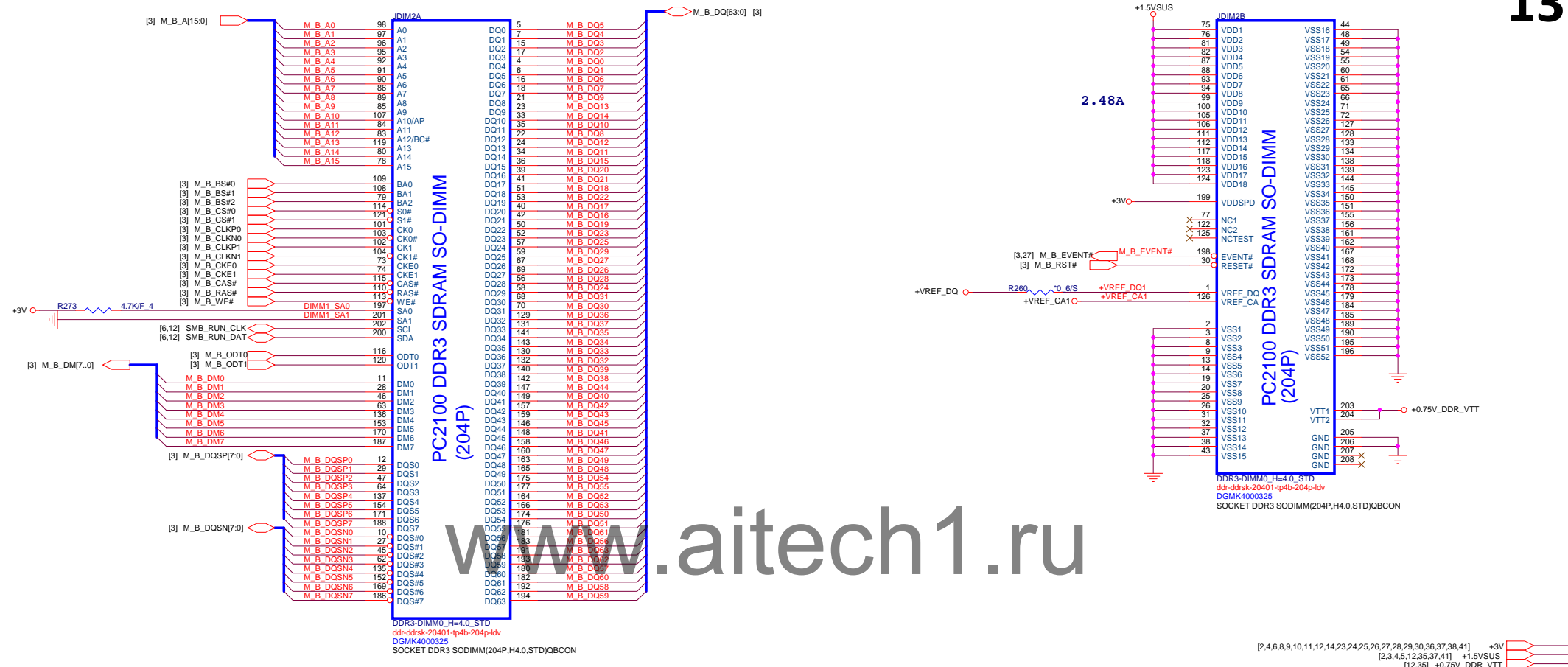


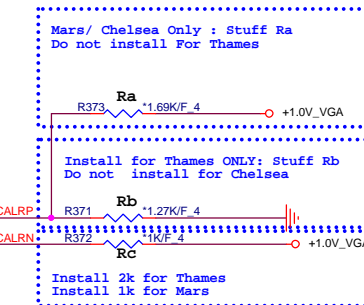
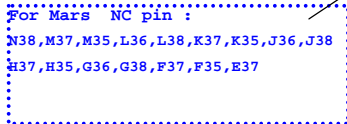
SCA_SCL pull high => EEPROM mode
SCA_SDA pull low => EEPROM Free mode

Address=0xA8

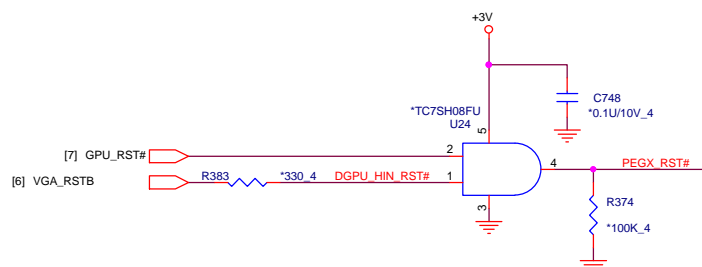








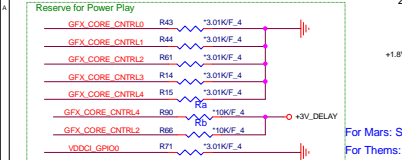
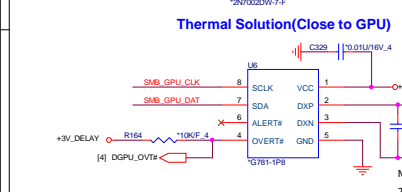
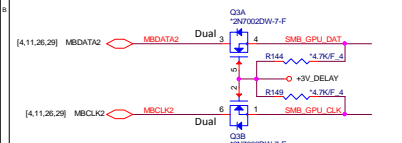
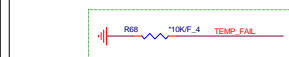
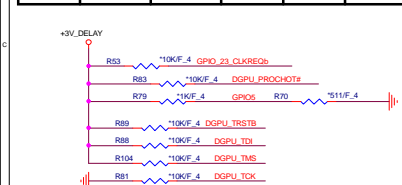
	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (V8GA)	84Mx16 #8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	84Mx16 #8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	84Mx16 #8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (V8GA)	128Mx16 #8, 900Mhz	H5TQ2G63DFR-11C
0100	Micron- D die	128Mx16 #8, 900Mhz	MT41J128M16JA-107G:D
0101	Samsung- C die	128Mx16 #8, 900Mhz	K4W2G1646C-BC11
0110	Reserve		
0111	Reserve		
1000	Reserve		
1001	Hynix- D (V8GA)	128Mx16 #8, 900Mhz	H5TQ2G63DFR-11C
1010			
1011			
1100			
1101			
1110			
1111			

GPIO30 GPIO12 GPIO16 GPIO20 GPIO15 Thames XT

PWR_CNTL4	PWR_CNTL3	PWR_CNTL2	PWR_CNTL1	PWR_CNTL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V



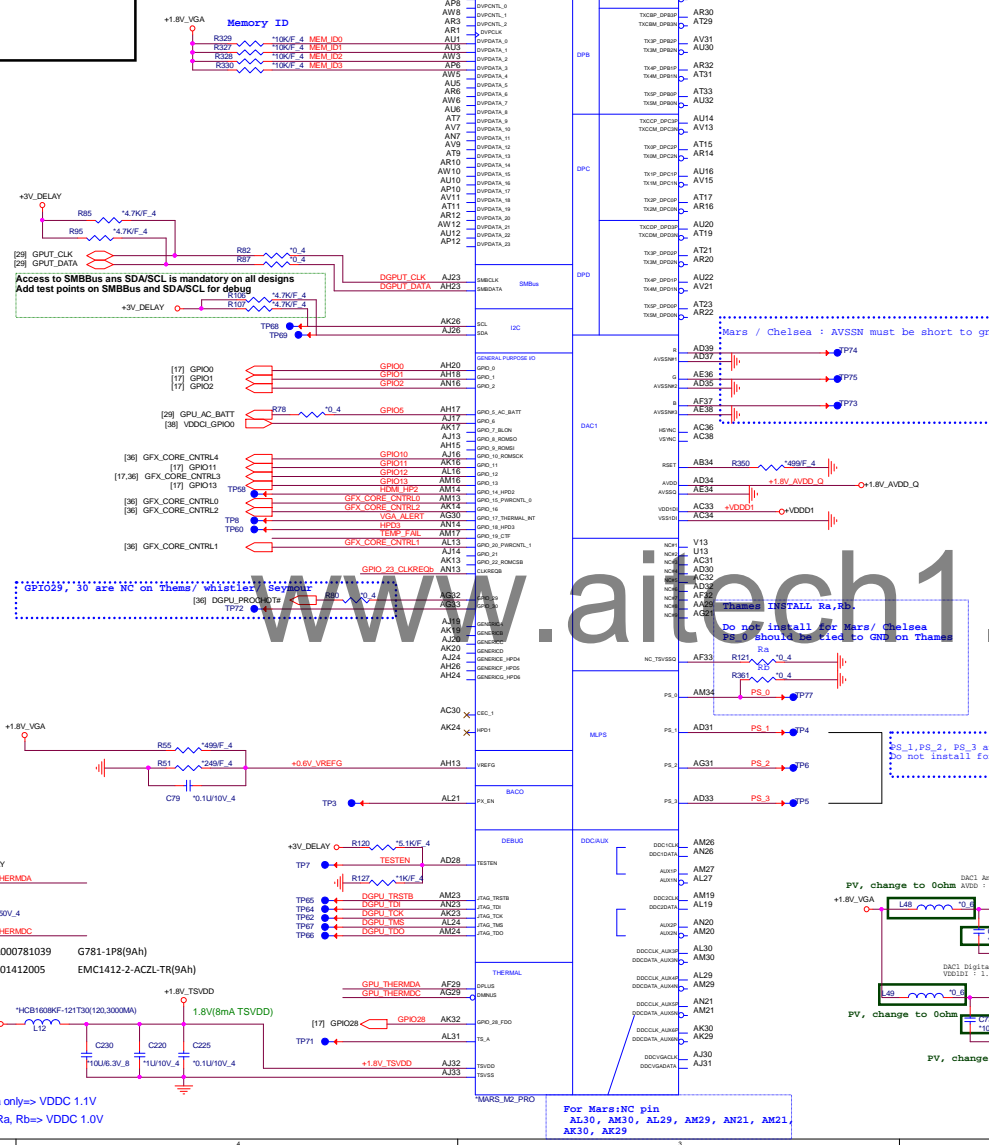
Reserve for Power Play

For Mars: Stuff Ra only => VDDC 1.1V

For Thems: Stuff Ra, Rb => VDDC 1.0V

For Mars only : AR1/AR6/AR3/AR6/AU8: all NC pin

For Mars only : DP A to D Port: all NC pin



MLPS Implementation

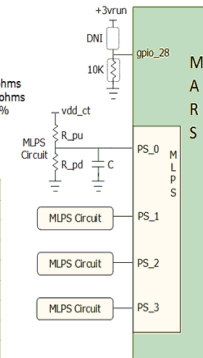
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

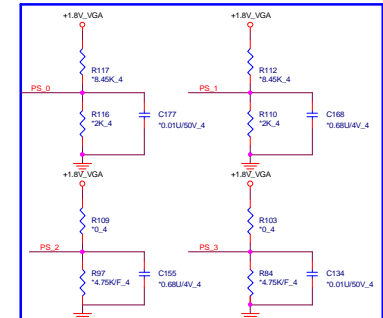
Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwrsv_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

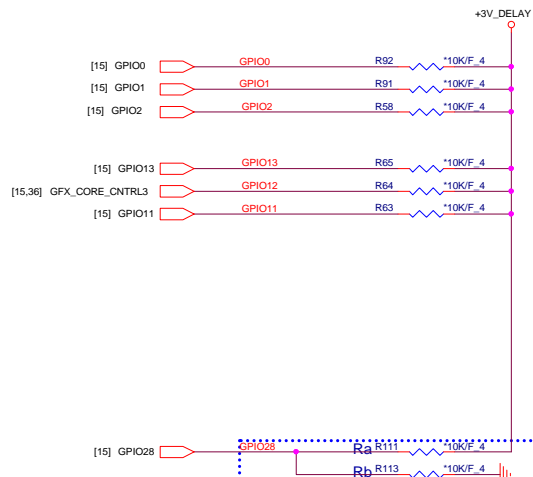
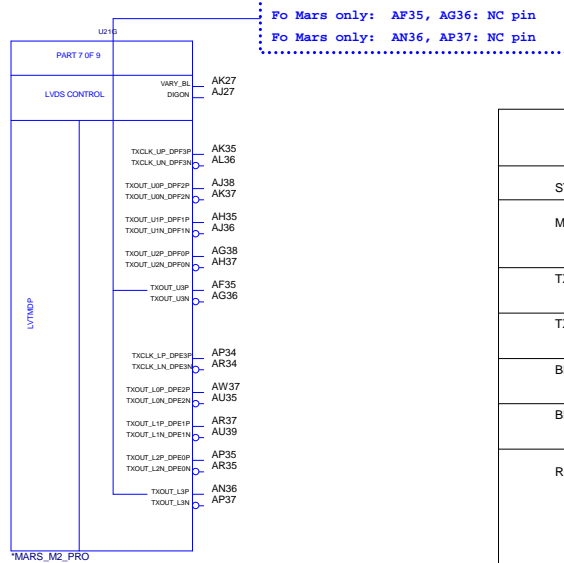
PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000



PROJECT : VOLKS Comal 14"
Quanta Computer Inc.
Docu: Mars_Main & GND
Date: Thursday, September 20, 2012 15:00
Rev: 1A

Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

[illegible]



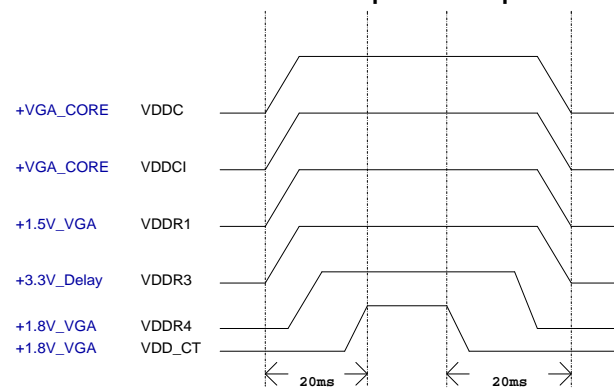
Memory Aperture size

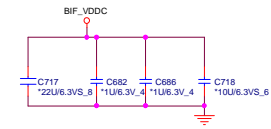
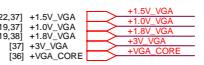
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DEFAULTS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET																						
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting																		
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X																		
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X																		
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X																		
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1																		
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0																		
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type <table><tr><td>100 - 512Kbit</td><td>M25P16A</td><td>(STD)</td></tr><tr><td>101 - 2Mbit</td><td>M25P32A</td><td>(STD)</td></tr><tr><td>101 - 2Mbit</td><td>M25P40</td><td>(STD)</td></tr><tr><td>101 - 8Mbit</td><td>M25P80</td><td>(STD)</td></tr><tr><td>101 - 512Kbit</td><td>Fm25LV512</td><td>(Chingis)</td></tr><tr><td>101 - 1Mbit</td><td>Fm25LV010</td><td>(Chingis)</td></tr></table>	100 - 512Kbit	M25P16A	(STD)	101 - 2Mbit	M25P32A	(STD)	101 - 2Mbit	M25P40	(STD)	101 - 8Mbit	M25P80	(STD)	101 - 512Kbit	Fm25LV512	(Chingis)	101 - 1Mbit	Fm25LV010	(Chingis)	XXX
100 - 512Kbit	M25P16A	(STD)																				
101 - 2Mbit	M25P32A	(STD)																				
101 - 2Mbit	M25P40	(STD)																				
101 - 8Mbit	M25P80	(STD)																				
101 - 512Kbit	Fm25LV512	(Chingis)																				
101 - 1Mbit	Fm25LV010	(Chingis)																				
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X																		
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX																		
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X																		
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0																		
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX																		

Power Up/Down Sequence

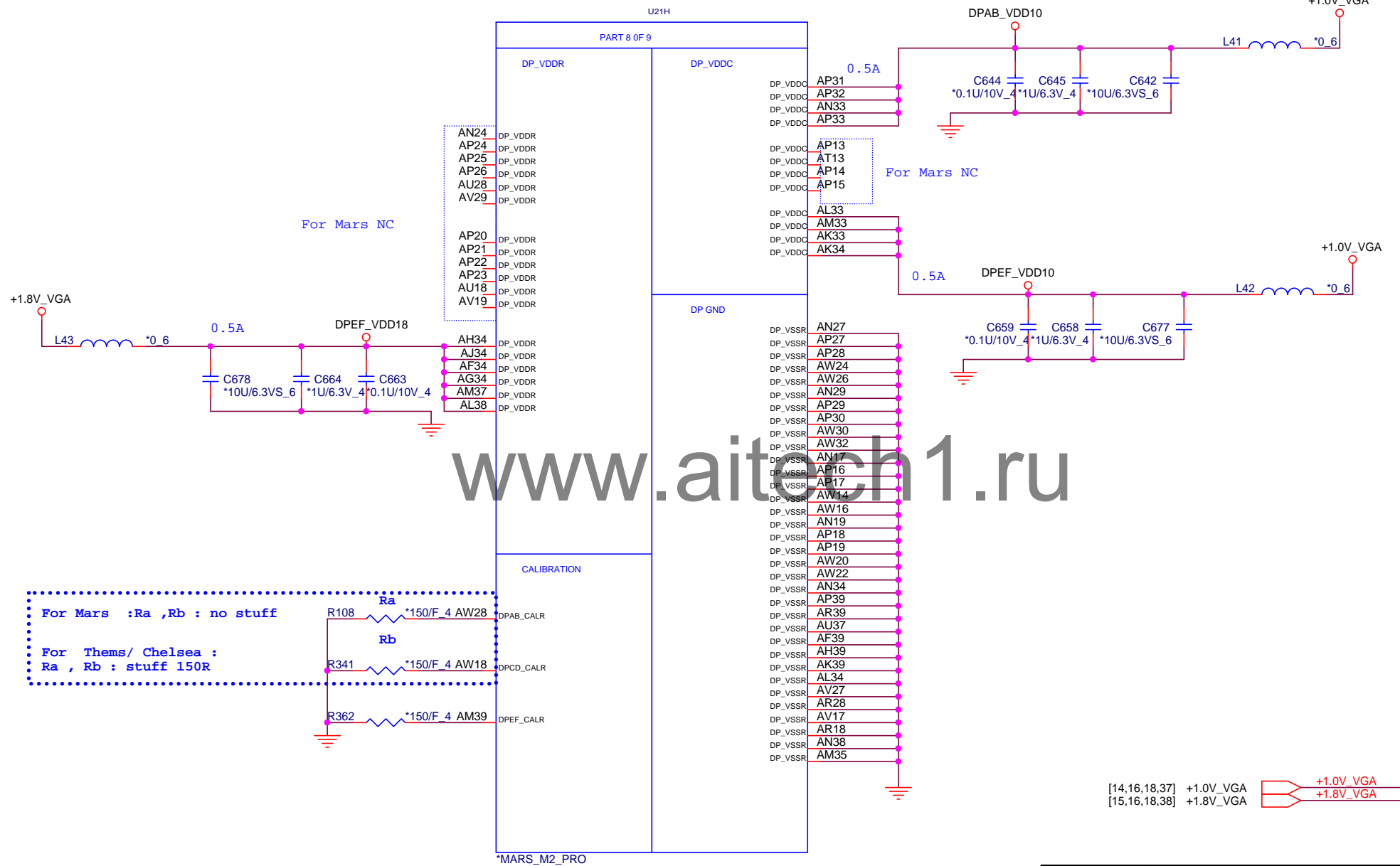




2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)



Size Custom	Document Number Mars_Power & BACO	Rev 1/
Date: Thursday, September 20, 2012		Sheet 18 of 42

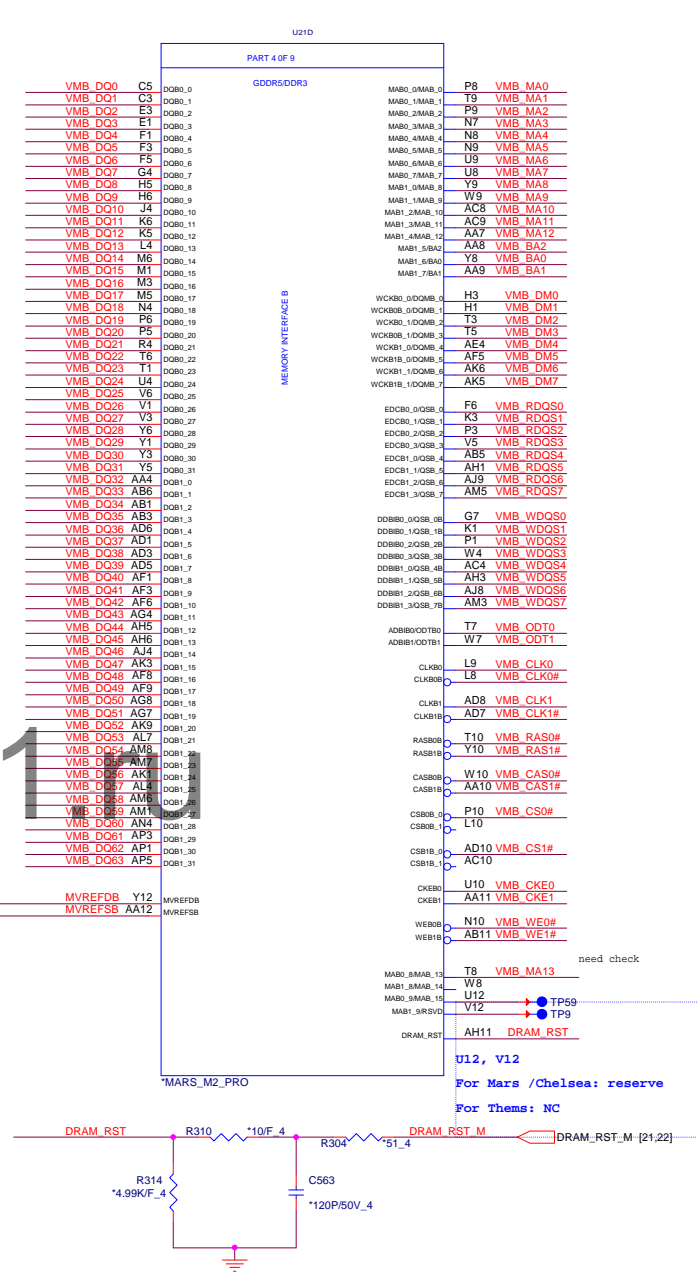
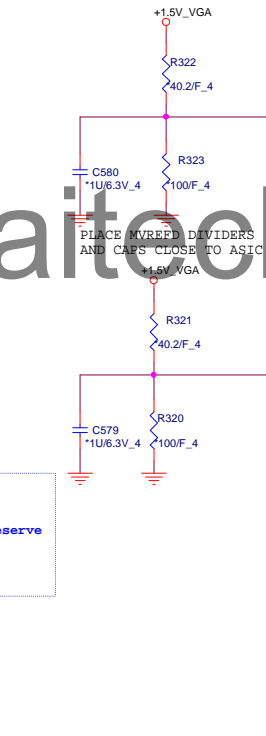
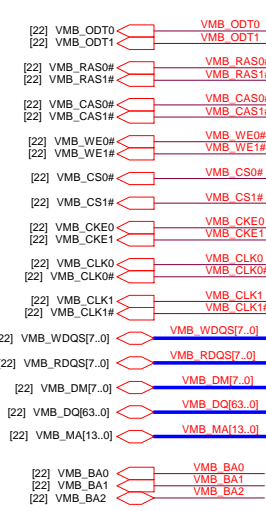
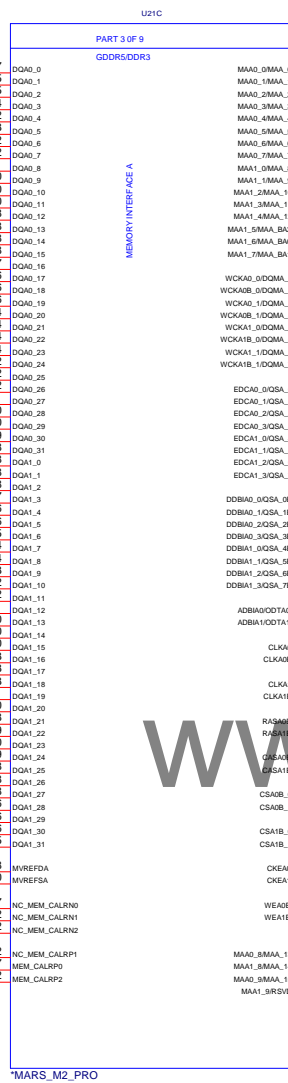
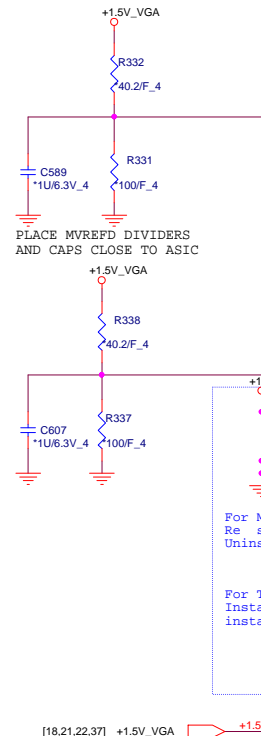
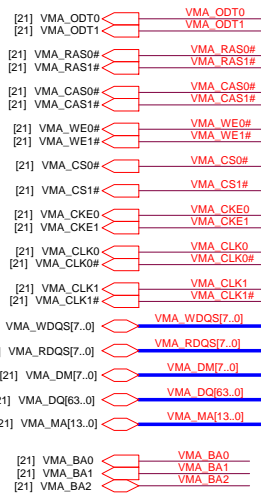


[14,16,18,37] +1.0V_VGA
[15,16,18,38] +1.8V_VGA



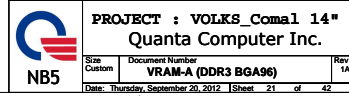
PROJECT : VOLKS_Coma1 14"
Quanta Computer Inc.

Size Custom	Document Number Mars_DP Powers	Rev 1A
Date: Thursday, September 20, 2012		Sheet 19 of 42

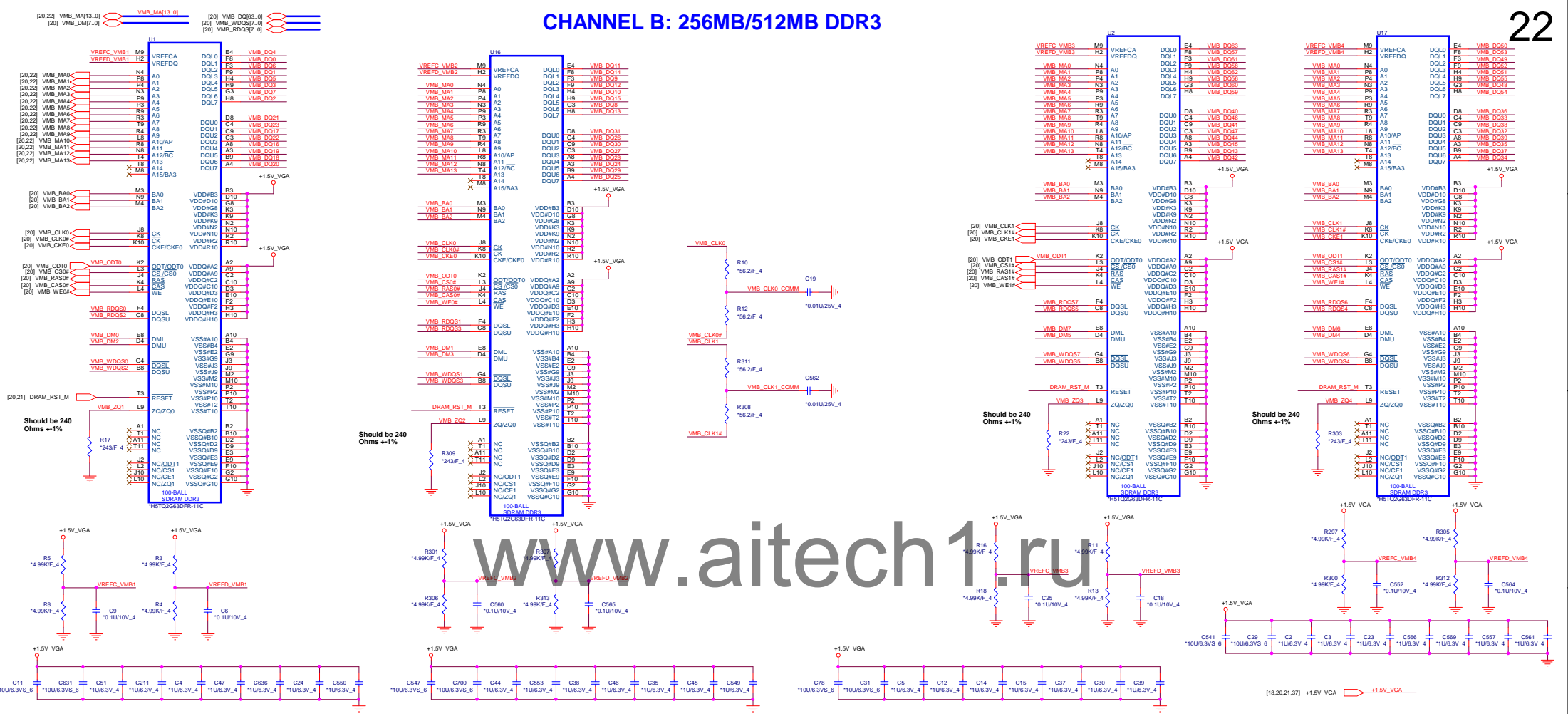


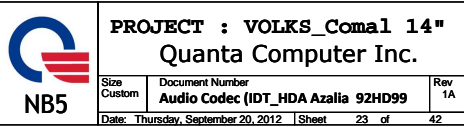
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars_MEM_Interface	1A
Date: Thursday, September 20, 2012	Sheet 20 of 42	



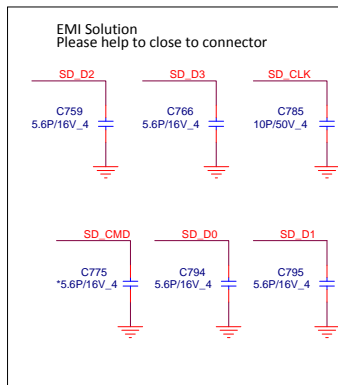
CHANNEL B: 256MB/512MB DDR3



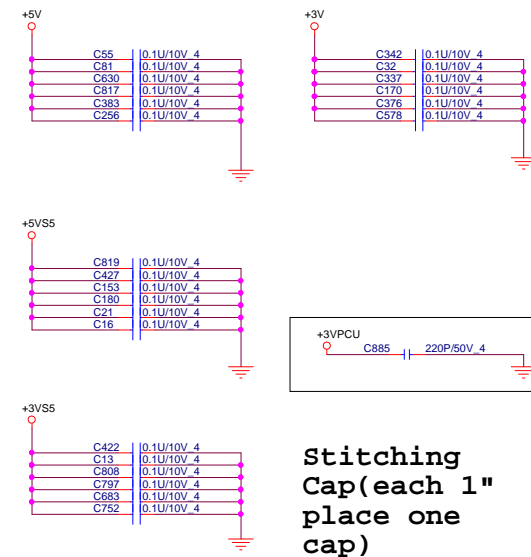
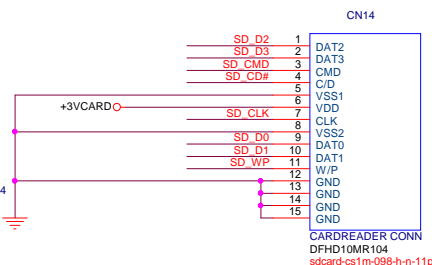


SD / MMC

EMI Solution
Please help to close to connector



Close to chip pin

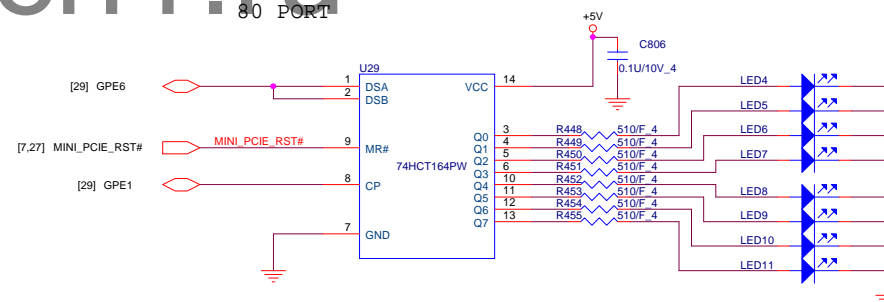
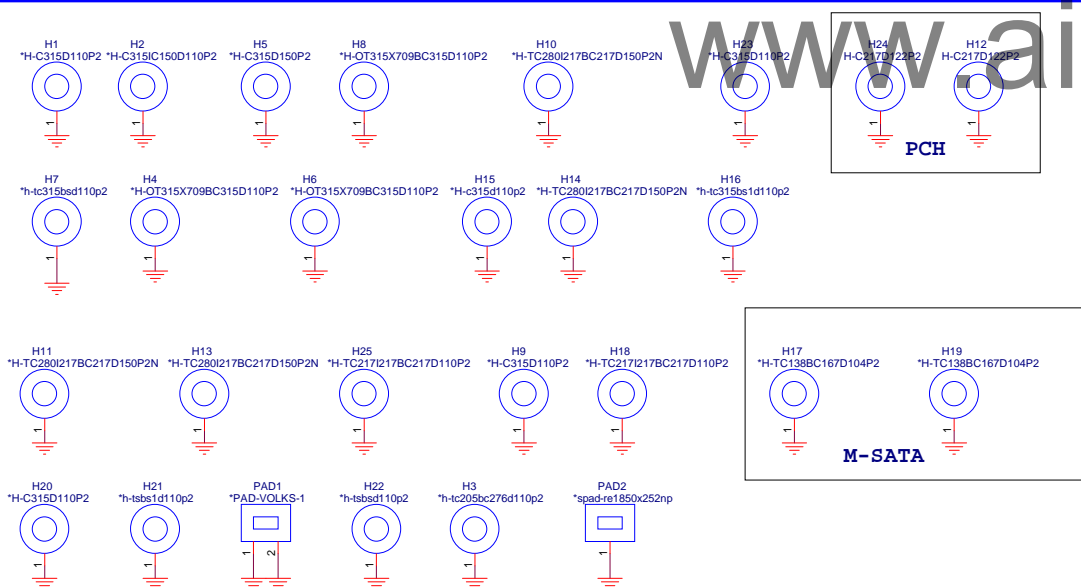


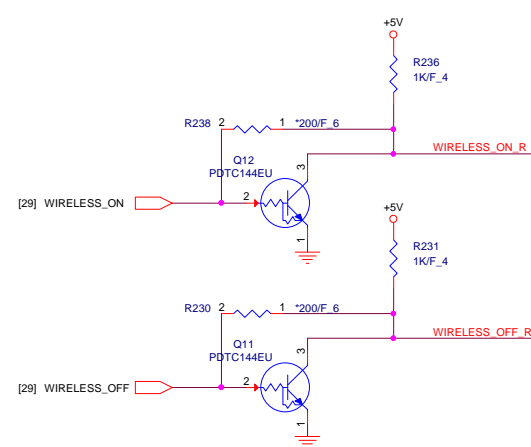
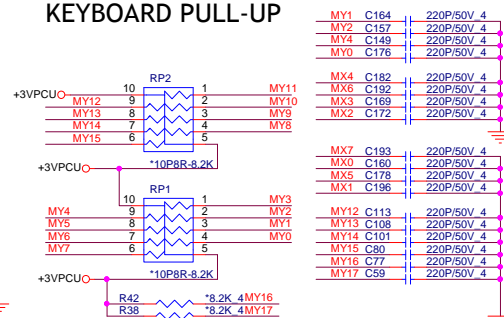
Stitching
Cap(each 1"
place one
cap)

EMI/ESD

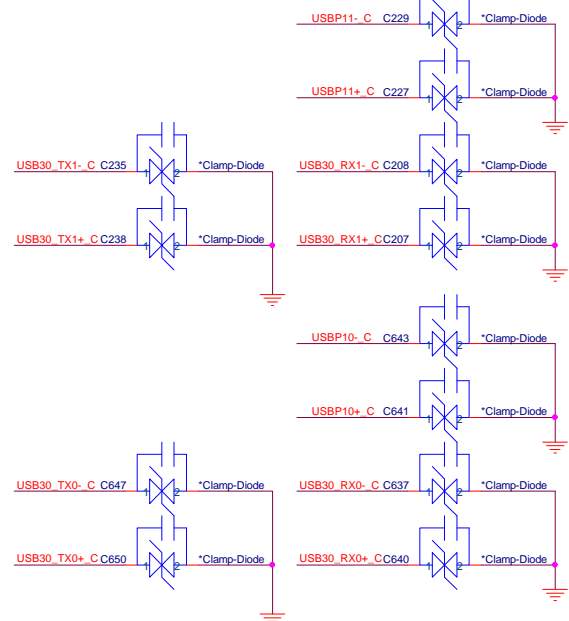
Note:

1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin1
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

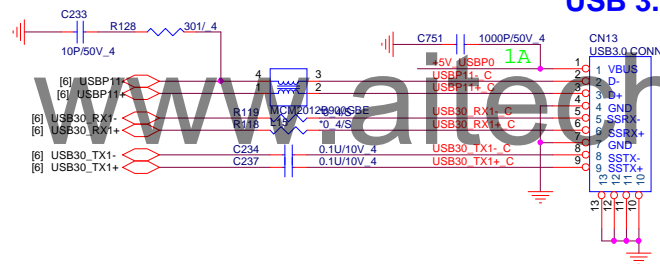




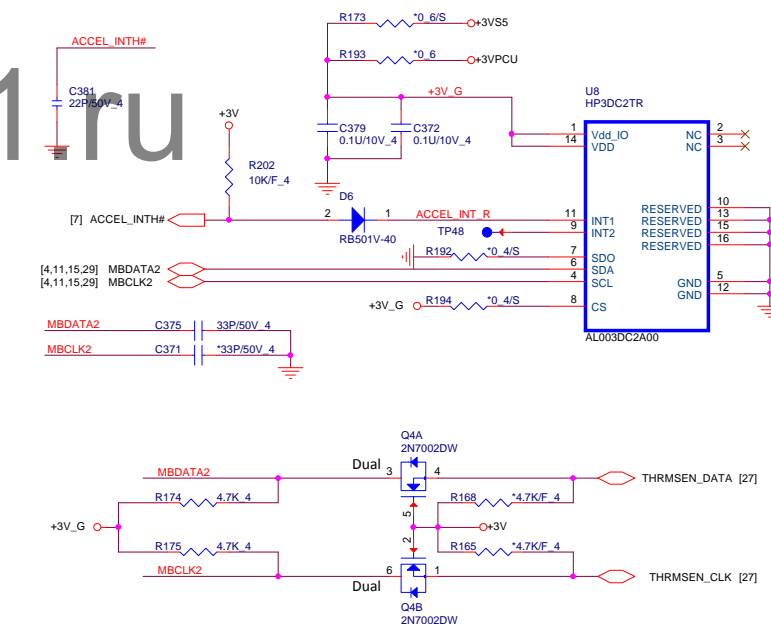
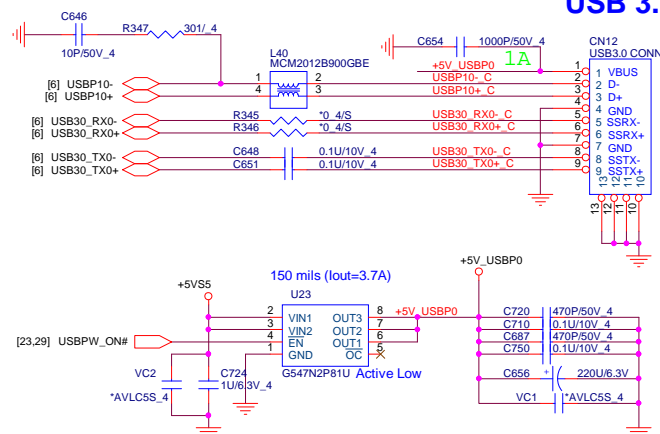
Accelerometer Sensor



USB 3.0

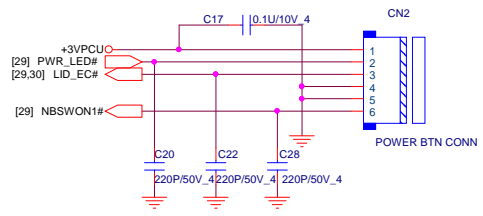


USB 3.0

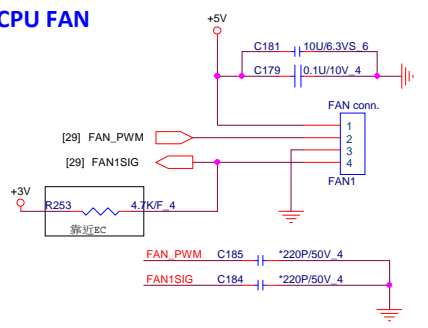


Power Button Connector

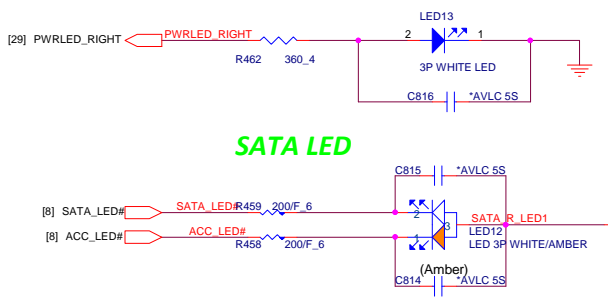
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



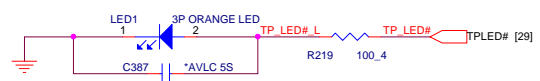
CPU FAN



LED Status

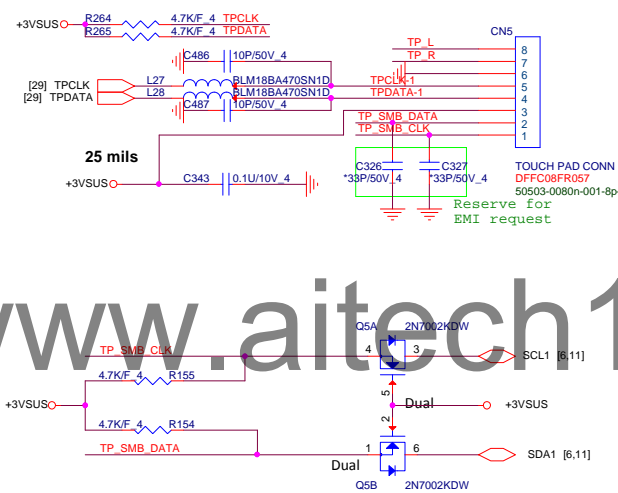
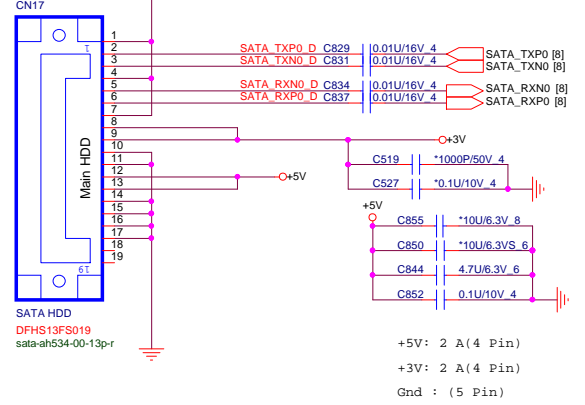


14 "TP LED

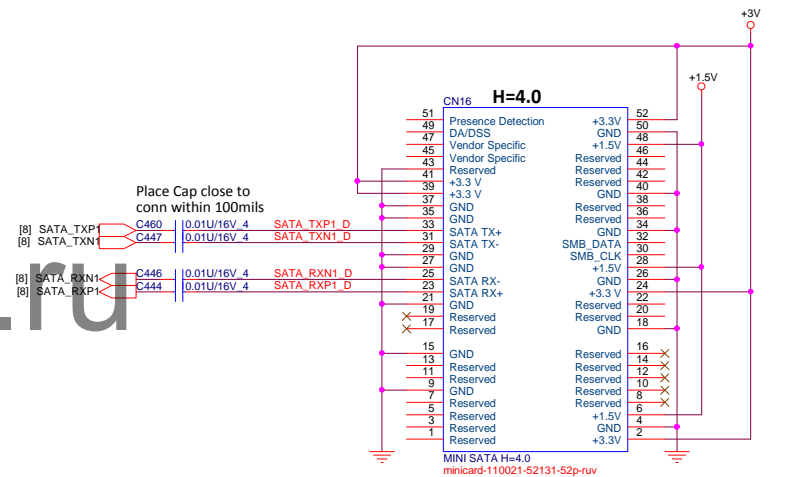


SATA HDD Connector(Cable type)

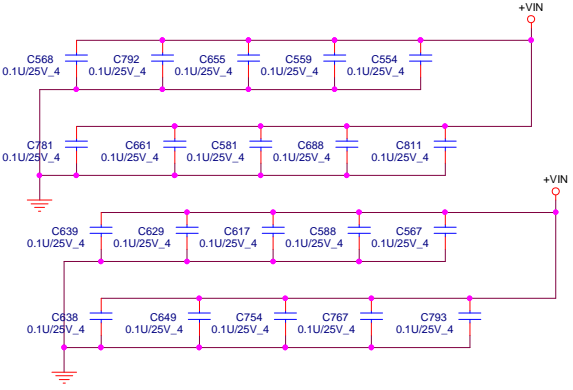
Bypass CAP close conn



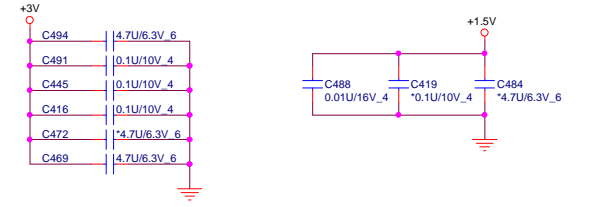
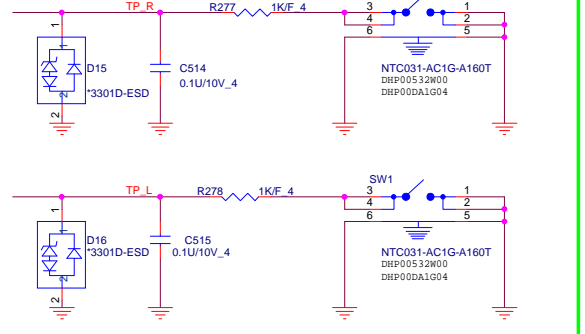
Mini PCI-E Card 2- Full size mSATA



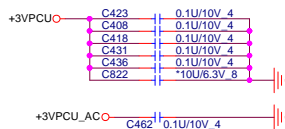
+VIN Cap



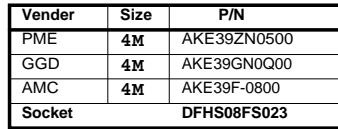
TP for 14"



+3V R235 *0_4/S KBC_P+3V

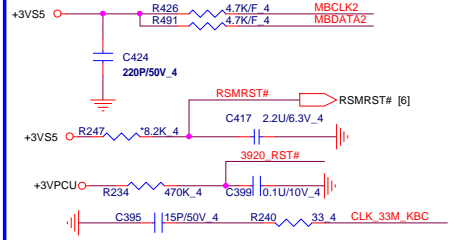
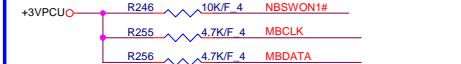
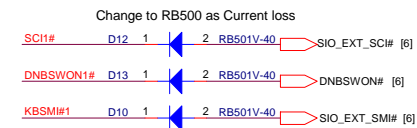
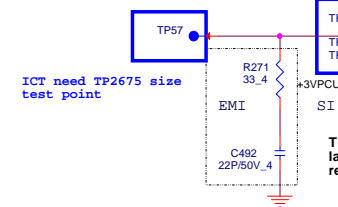
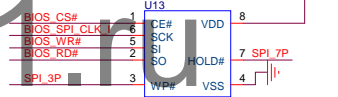


+3VPCU CAP close to EC pin



Pin 1 to 8 of U13:

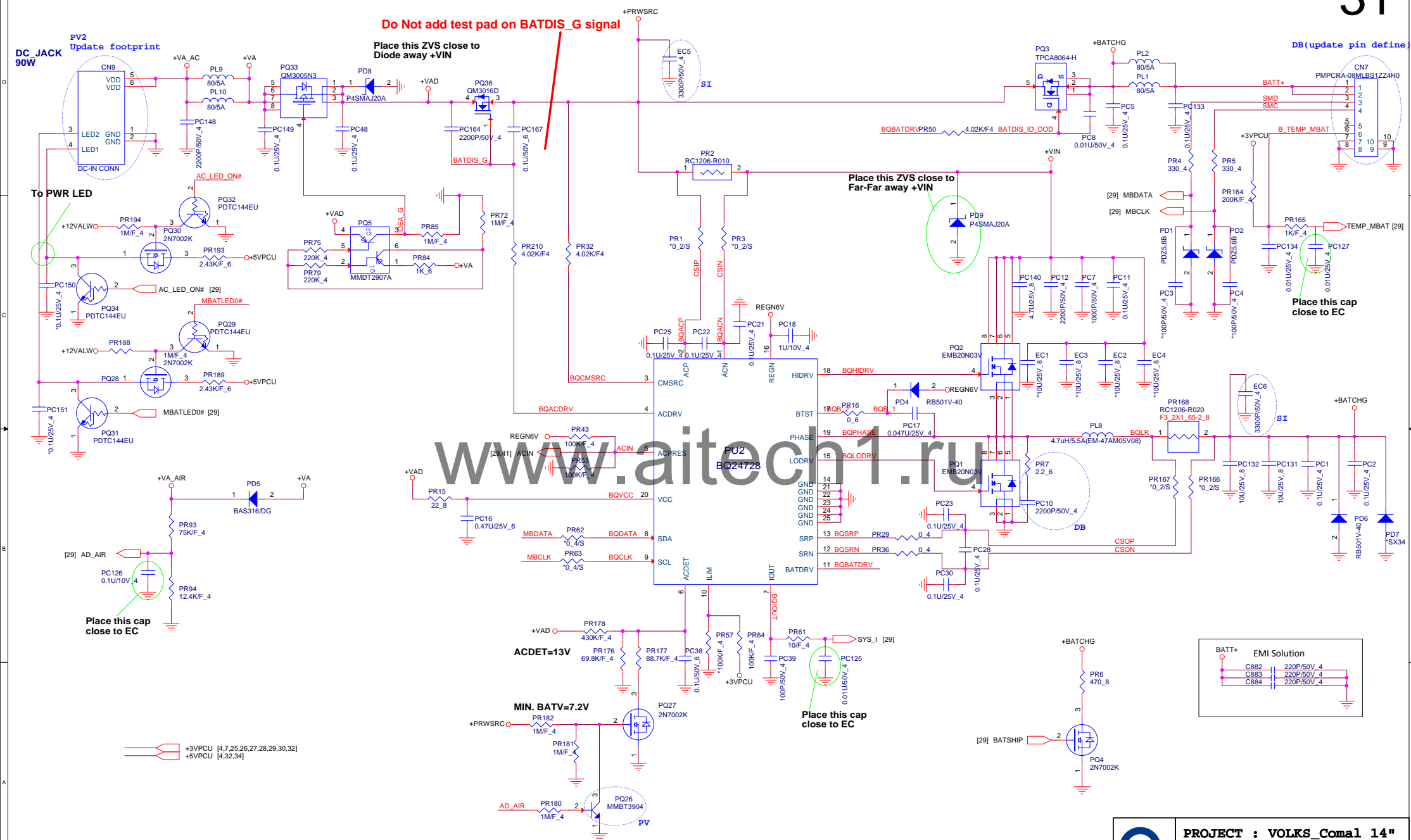
- Pin 1: BIOS_CS#
- Pin 2: BIOS_RD#
- Pin 3: SPI_3P
- Pin 4: WP#
- Pin 5: BIOS_WR#
- Pin 6: BIOS_SPI_CLK
- Pin 7: SPI_7P
- Pin 8: VDD

[illegible]

+3VPCU 
Hi ==> DIS/SG
Low ==>UMA

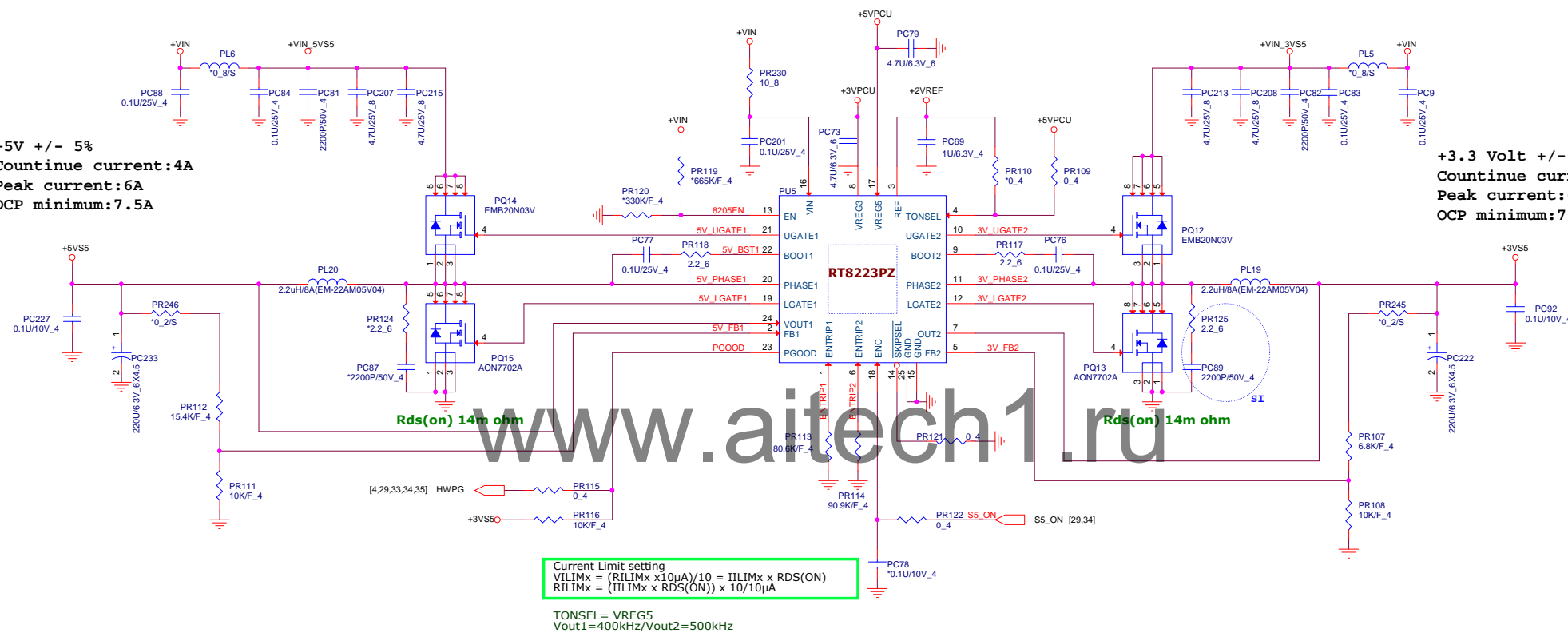


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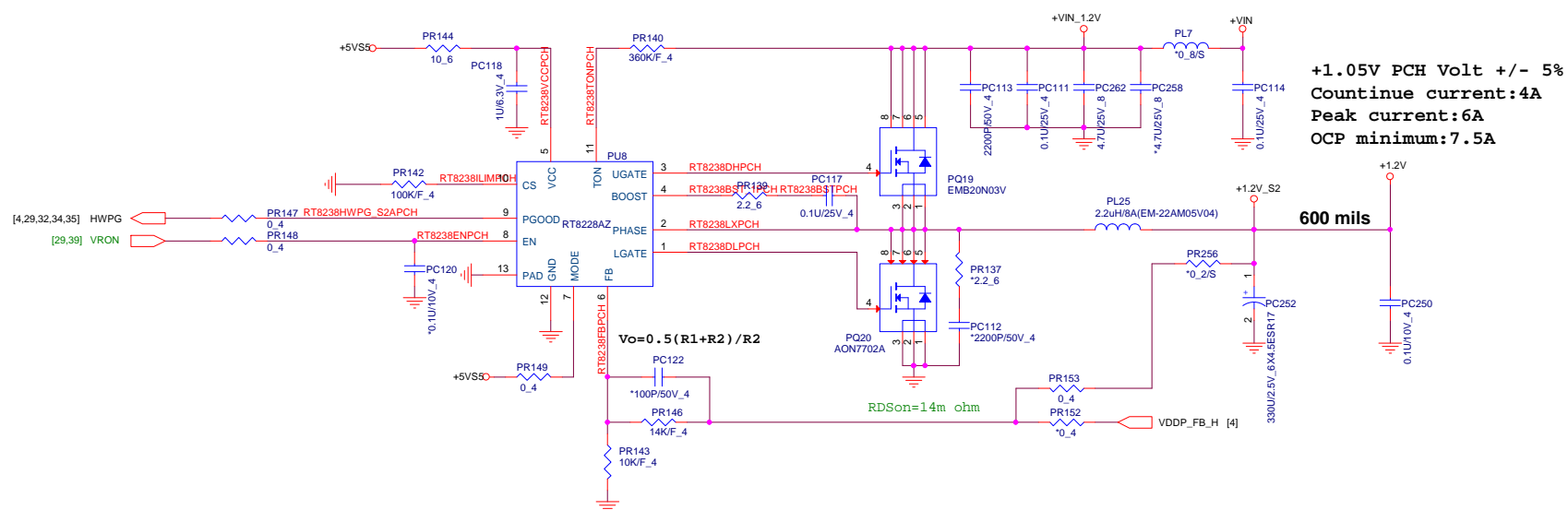


+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

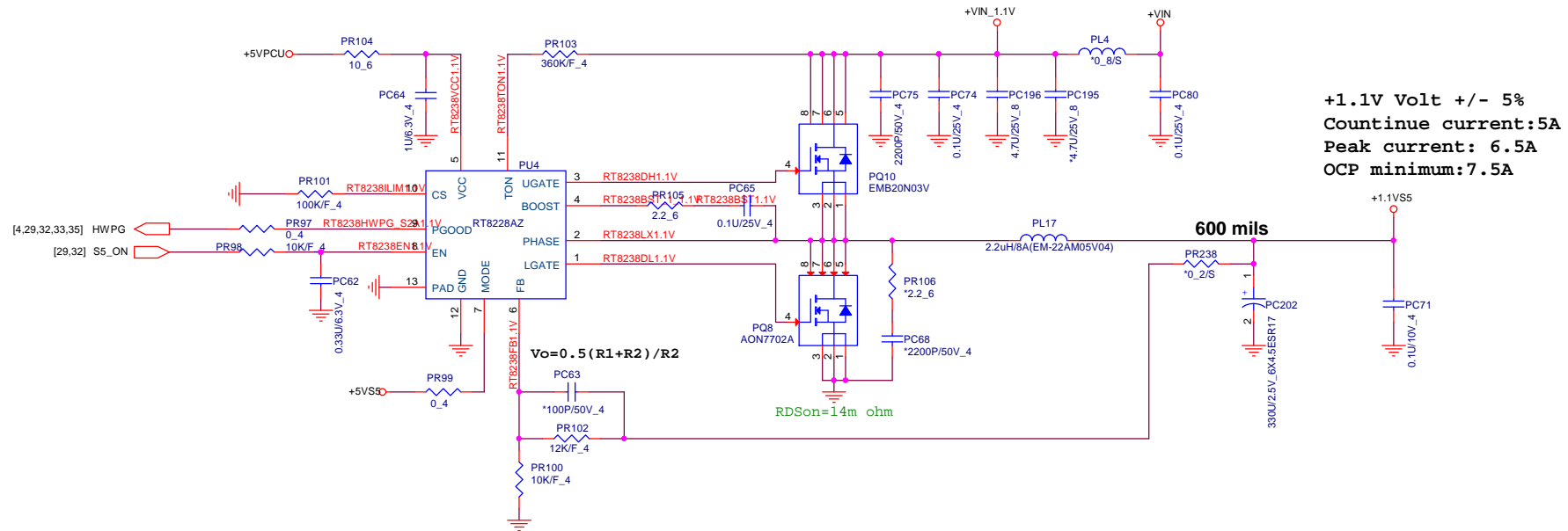
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



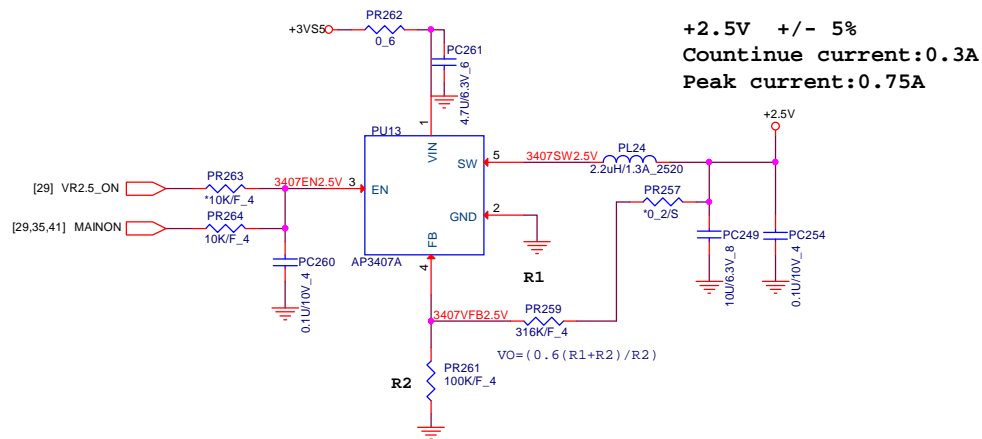
[28,30,31,33,34,35,36,37,38,40,41] +VIN
 [6,8,9,10,25,26,27,29,34,36,37,41] +3VSS
 [23,25,26,33,34,35,36,38,39,40,41] +5VSS
 [4,7,25,26,27,28,29,30,31] +3VPCU



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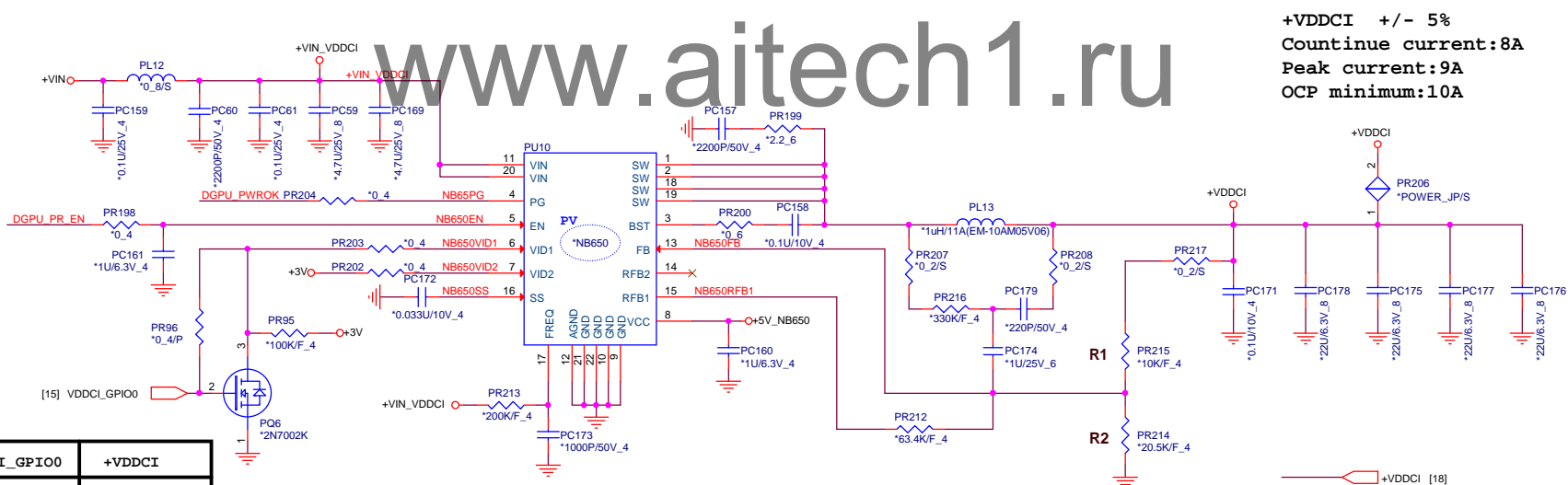
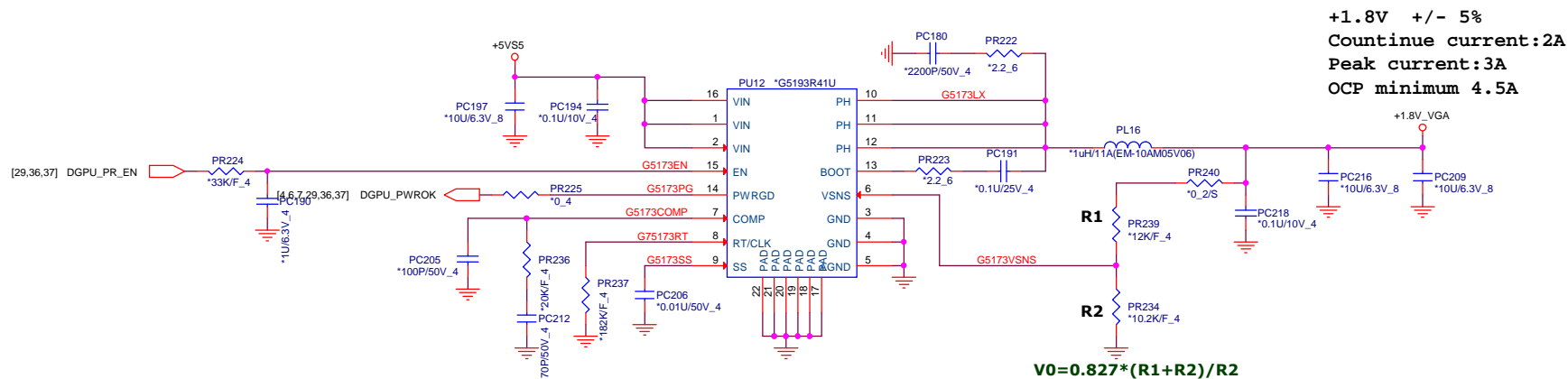
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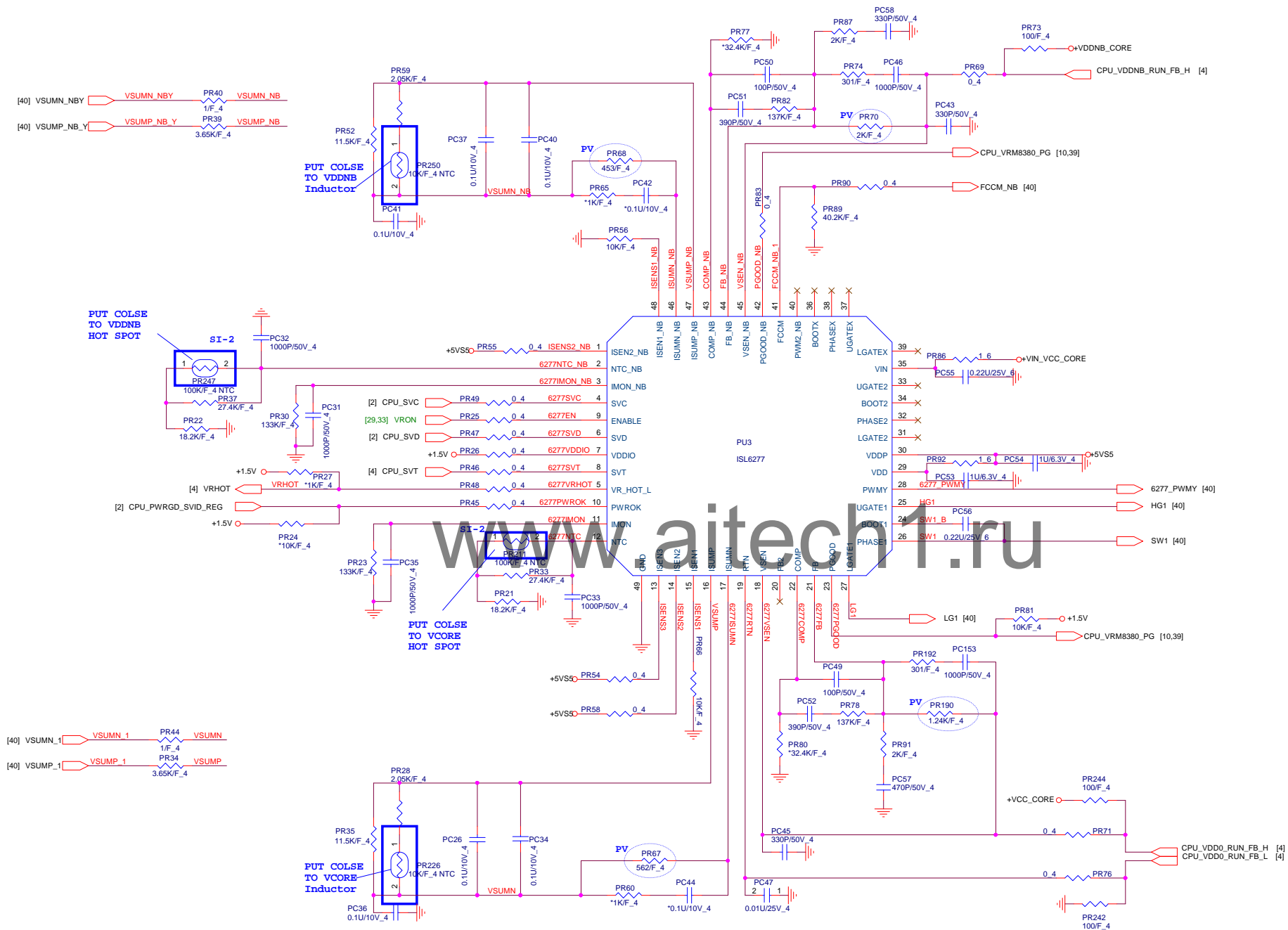
VDDCI_GPI01	VDDCI_GPI00	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

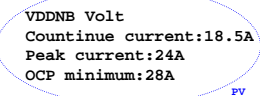
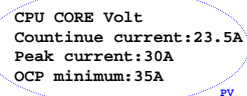


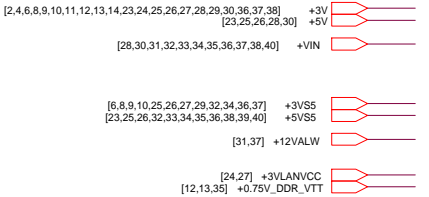
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